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10/675,841	09/30/2003	Peter B. Criswell	RA5635	6910

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EXAMINER	
DARE, RYAN A	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,841	CRISWELL, PETER B.	
	Examiner	Art Unit	
	RYAN DARE	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-16,19-29,36 and 37* is/are rejected.

7)☒ Claim(s) *3,4,17,18 and 30-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-2, 6-16, 19-29, and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis et al., US Patent 4,201,337, in view of Usami, US Patent 6,205,516.

1. With respect to claim 1, Lewis et al. teach a control system, comprising:

a storage device to store data signals, the mode designator to select a first or second mode of operation, in the Abstract, where the first mode is the byte parity mode and the second mode is the ECC mode, and the embodiment described in col. 3, lines 29-40, where the examiner is considering the main memory 14 as the storage device for storing the data signals.

a circuit coupled to the storage device to receive as control signals predetermined ones of the data signals, the control signals to control operations of the circuit when the circuit is operating in the first mode, in col. 1, lines 37-41, and col. 2, lines 29-40 where the examiner is considering the EDC circuit as the circuit coupled to the storage device; and

Error Correction Code (ECC) logic coupled to the storage device to interpret the predetermined ones of the data signals as ECC check bits to detect errors in the data signals when the circuit is operating in the second mode, in the Abstract (ECC mode) and col. 3, lines 29-40.

The system of Lewis teaches a circuit that can be operated in 2 different modes, depending on an input to the ECC/BP input in the EDC circuit. Lewis remains silent on where this signal is supplied from and if and how it is stored. Usami resolves this deficiency, teaching a programmable mode register which acts as a storage device to store a mode designator, as required by the present claim, in col. 9, lines 45-62.

2. It would have been obvious to one of ordinary skill in the art, having the teachings of Lewis and Usami before him at the time the invention was made, to modify the control system of Lewis with the control system of Usami in order to set a desired operation mode specific to data received, as taught by Usami in col. 2, lines 29-34.

3. With respect to claim 2, Lewis et al. teach the system of Claim 1, wherein the storage device is a memory having multiple addressable storage locations, each storing a different respective set of data signals, in fig. 1, main memory 14, and col. 3, lines 29-40.

4. With respect to claim 6, Lewis et al. teach the system of claim 1, wherein the circuit includes logic to provide one or more functions of an instruction processor, in col. 2, line 68 through col.3, line 2.

5. With respect to claim 7, Lewis et al. teach the system of Claim 1, and further including a programmable storage device coupled to the circuit to select the predetermined ones of the data signals, in fig. 1, Control Store 18.

6. With respect to claim 8, Lewis et al. teach the system of Claim 1, and further including at least one parity circuit coupled to the storage device to determine whether a parity error occurred on any of a predetermined set of the data signals, in col. 4, lines 16-18.

7. With respect to claim 9, Lewis et al. teach the system of Claim 8, wherein the at least one parity circuit includes a circuit to determine whether a parity error occurred on the predetermined set of the data signals when the circuit is operating in the second mode, in col. 4, lines 16-18. The second mode is byte parity mode.

8. With respect to claim 10, Lewis et al. teach the system of Claim 1, wherein the ECC logic is coupled to ECC complement logic to correct errors in the data signals that are detected by the ECC logic when operating in the second mode, in col. 1, lines 48-59.

9. With respect to claim 11, Lewis et al. teach the system of Claim 10, and further including logic coupled to the ECC complement logic to provide data signals to the circuit for use as control signals after any errors detected by the ECC logic have been corrected, in col. 1, lines 34-42.

10. With respect to claims 12-13 and 19-24, these claims describe a method that corresponds to the system as claimed in claims 1-2 and 6-11, and is therefore rejected using similar logic.

11. With respect to claim 14, Lewis et al. teach the method of Claim 13, wherein the storage device is a memory, and wherein the first and second data signals are stored at a same addressable location within the memory, in col. 3, lines 29-40.

12. With respect to claim 15, Lewis et al. teach the method of Claim 14, wherein multiple memory addresses each stores different respective first and second data signals, in col. 3, lines 29-40.

13. With respect to claim 16, Lewis et al. teach the method of claim 15, and further including using the first data signals to generate a next address for addressing the memory when operating in the first mode of operation, in col. 2, line 66 through col. 3, line 8.

14. With respect to claim 25, Lewis et al. teach the method of Claim 24, and further including:

servicing any error detected by the ECC signals at a time that is optimal for the digital system, in col. 3, lines 35-37 where the ECC bits are stored in the memory for use later; and

servicing any error detected using the parity bits substantially immediately, in col. 3, lines 38-40.

15. With respect to claims 26-29 and 36-37, these claims describe a system that corresponds to various aspects of the system claimed in claims 1-2, 6-11 and the method claimed in claims 12-15 and 19-25 and is therefore rejected using similar logic.

Allowable Subject Matter

16. Claims 3-4, 17-18 and 30-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter: No prior art teaches a storage device to store data signals wherein each of the addressable storage locations of the storage device stores data and a respective mode indicator to whether the circuit operates in the first or the second mode, the first mode interpreting data signals as control signals, and the second mode interpreting the data signals as error check signals.

Response to Arguments

18. Applicant's arguments, see Appeal Brief, filed 2/27/07, with respect to the rejection(s) of claim(s) 1-4 and 6-37 under 35 USC 102(b) have been fully considered and are persuasive. Therefore, the finality of the last office action has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made of the claims above in view of Usami.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN DARE whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

/Ryan Dare/
April 27, 2008